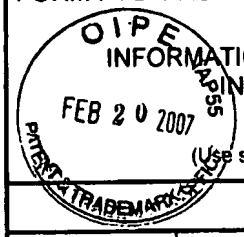
CUSTOMER NO.: 27623

Sheet 1 of 1

FORM PTO-1449



INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
US 20 02.1052-2	10/635,198
Applicant	
Rolf HARJUNG	
Filing Date	**Group Art Unit**
August 6, 2003	2125

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.)

CO	Arunachalam, Ravishankar et al. "CMOS Gate Delay Models for General RLC Loading".
	Proceedings of the 1997 International conference on Computer Design (ICCD '97),
CO	0-8186-8206-X/97, 1997 IEEE, pp. 1-7.
	Dartu, Florentin et al. "A Gate-Delay Model for High-Speed CMOS Circuits". 31st ACM/IEEE
CO	Design Automation Conference, pp. 576-580, 1994.

EXAMINER	DATE CONSIDERED
	4/5/07

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.